LAMPIRAN 1
LISTING PROGRAM

/***
****

This program was produced by the

CodeWizardAVR V2.05.0 Professional

Automatic Program Generator

http://www.hpinfotech.com

Project :

Version :

Date : 7/10/2014

Author : NeVaDa

Company :

Comments:

Chip type : ATmega16

Program type : Application

AVR Core Clock frequency: 11.059200 MHz

Memory model : Small

External RAM size : 0

```
Data Stack size        : 128
*************************************************
***/

#include <mega16.h>
#include <stdlib.h>
#include <delay.h>

// Alphanumeric LCD Module functions
#include <alcd.h>

// Declare your global variables here
unsigned char buff[16];
float v;

void main(void)
{
// Declare your local variables here

// Input/Output Ports initialization
// Port A initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In
Func2=In Func1=In Func0=In
```

```
// State7=T State6=T State5=T State4=T State3=T State2=T
State1=T State0=T
PORTA=0x00;
DDRA=0x00;

// Port B initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In
Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T State3=T State2=T
State1=T State0=T
PORTB=0x00;
DDRB=0x00;

// Port C initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In
Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T State3=T State2=T
State1=T State0=T
PORTC=0x00;
DDRC=0x00;

// Port D initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In
Func2=In Func1=In Func0=In
```

```
// State7=T State6=T State5=T State4=T State3=T State2=T
State1=T State0=T
PORTD=0x00;
DDRD=0x00;

// Timer/Counter 0 initialization
// Clock source: System Clock
// Clock value: Timer 0 Stopped
// Mode: Normal top=0xFF
// OC0 output: Disconnected
TCCR0=0x00;
TCNT0=0x00;
OCR0=0x00;

// Timer/Counter 1 initialization
// Clock source: T1 pin Falling Edge
// Mode: Normal top=0xFFFF
// OC1A output: Discon.
// OC1B output: Discon.
// Noise Canceler: Off
// Input Capture on Falling Edge
// Timer1 Overflow Interrupt: Off
// Input Capture Interrupt: Off
// Compare A Match Interrupt: Off
```

```
// Compare B Match Interrupt: Off
TCCR1A=0x00;
TCCR1B=0x06;
TCNT1H=0x00;
TCNT1L=0x00;
ICR1H=0x00;
ICR1L=0x00;
OCR1AH=0x00;
OCR1AL=0x00;
OCR1BH=0x00;
OCR1BL=0x00;

// Timer/Counter 2 initialization
// Clock source: System Clock
// Clock value: Timer2 Stopped
// Mode: Normal top=0xFF
// OC2 output: Disconnected
ASSR=0x00;
TCCR2=0x00;
TCNT2=0x00;
OCR2=0x00;

// External Interrupt(s) initialization
// INT0: Off
```

```
// INT1: Off
// INT2: Off
MCUCR=0x00;
MCUCSR=0x00;

// Timer(s)/Counter(s) Interrupt(s) initialization
TIMSK=0x00;

// USART initialization
// USART disabled
UCSRB=0x00;

// Analog Comparator initialization
// Analog Comparator: Off
// Analog Comparator Input Capture by Timer/Counter 1: Off
ACSR=0x80;
SFIOR=0x00;

// ADC initialization
// ADC disabled
ADCSRA=0x00;

// SPI initialization
// SPI disabled
```

```
SPCR=0x00;

// TWI initialization
// TWI disabled
TWCR=0x00;

// Alphanumeric LCD initialization
// Connections specified in the
// Project|Configure|C Compiler|Libraries|Alphanumeric LCD
menu:
// RS - PORTC Bit 0
// RD - PORTC Bit 1
// EN - PORTC Bit 2
// D4 - PORTC Bit 4
// D5 - PORTC Bit 5
// D6 - PORTC Bit 6
// D7 - PORTC Bit 7
// Characters/line: 16
lcd_init(16);
lcd_clear();
lcd_gotoxy(0,0);
lcd_putsf("Anemometer");
lcd_gotoxy(0,1);
lcd_putsf("By Megan");
```

```
delay_ms(5000);

while (1)
      {
      // Place your code here
      TCNT1H=0x00;
      TCNT1L=0x00;
      TCCR1A=0x00;
      TCCR1B=0x06;
      delay_ms(1000);
      TCCR1B=0;
      v=((float)0.5652*TCNT1);
      ftoa(v,2,buff);
      lcd_clear();
      lcd_gotoxy(0,0);
      lcd_putsf("Anemometer");
      lcd_gotoxy(0,1);
      lcd_putsf("v = ");
      lcd_puts(buff);
      lcd_putsf(" km/jam");
      };
}
```

Features

- High-performance, Low-power Atmel® AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 × 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 16 Kbytes of In-System Self-programmable Flash program memory
  - 512 Bytes EEPROM
  - 1 Kbyte Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C[1]
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC
    8 Single-ended Channels
    7 Differential Channels in TQFP Package Only
    2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF
- Operating Voltages
  - 2.7V - 5.5V for ATmega16L
  - 4.5V - 5.5V for ATmega16
- Speed Grades
  - 0 - 8 MHz for ATmega16L
  - 0 - 16 MHz for ATmega16
- Power Consumption @ 1 MHz, 3V, and 25°C for ATmega16L
  - Active: 1.1 mA
  - Idle Mode: 0.35 mA
  - Power-down Mode: < 1 µA

8-bit AVR® Microcontroller with 16K Bytes In-System Programmable Flash

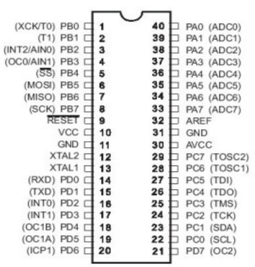
ATmega16
ATmega16L

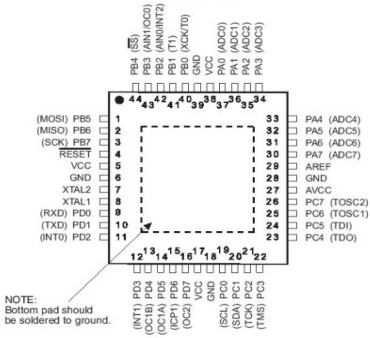
Summary

Rev. 2466TS–AVR–07/10

Pin Configurations

Figure 1. Pinout ATmega16





Disclaimer

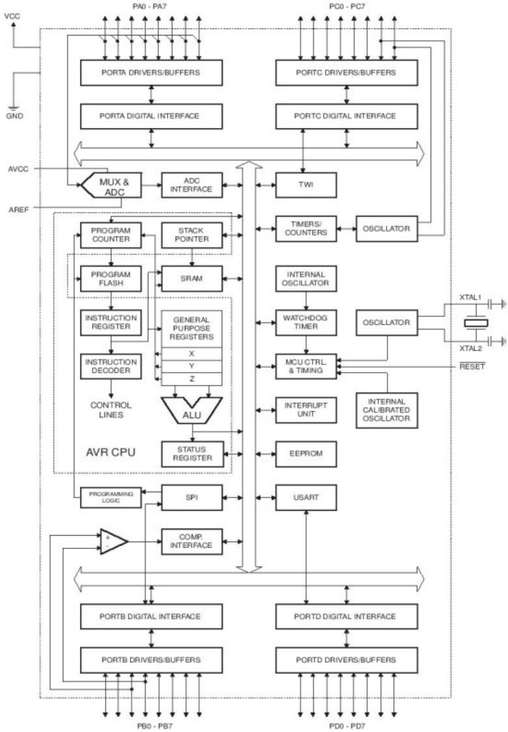
Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

Overview

The ATmega16 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega16 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 2. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega16 provides the following features: 16 Kbytes of In-System Programmable Flash Program memory with Read-While-Write capabilities, 512 bytes EEPROM, 1 Kbyte SRAM, 32 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, three flexible Timer/Counters with compare modes, Internal and External Interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain (TQFP package only), a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the USART, Two-wire interface, A/D Converter, SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next External Interrupt or Hardware Reset. In Power-save mode, the Asynchronous Timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega16 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega16 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Pin Descriptions

VCC Digital supply voltage.

GND Ground.

Port A (PA7..PA0) Port A serves as the analog inputs to the A/D Converter.

Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega16 as listed on page 58.

Port C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PC5(TDI), PC3(TMS) and PC2(TCK) will be activated even if a reset occurs.

Port C also serves the functions of the JTAG interface and other special features of the ATmega16 as listed on page 61.

Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega16 as listed on page 63.

$\overline{\text{RESET}}$

Reset Input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to generate a reset.

XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting Oscillator amplifier.

AVCC

AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

AREF

AREF is the analog reference pin for the A/D Converter.

Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	9
$3E ($5E)	SPH	–	–	–	–	–	SP10	SP9	SP8	12
$3D ($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	12
$3C ($5C)	OCR0	Timer/Counter0 Output Compare Register								85
$3B ($5B)	GICR	INT1	INT0	INT2	–	–	–	IVSEL	IVCE	48, 69
$3A ($5A)	GIFR	INTF1	INTF0	INTF2	–	–	–	–	–	70
$39 ($59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	85, 115, 133
$38 ($58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	86, 115, 133
$37 ($57)	SPMCR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	250
$36 ($56)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	180
$35 ($55)	MCUCR	SM2	SE	SM1	SM0	ISC11	ISC10	ISC01	ISC00	32, 68
$34 ($54)	MCUCSR	JTD	ISC2	–	JTRF	WDRF	BORF	EXTRF	PORF	41, 69, 231
$33 ($53)	TCCR0	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	83
$32 ($52)	TCNT0	Timer/Counter0 (8 Bits)								85
$31[1] ($51)[1]	OSCCAL	Oscillator Calibration Register								30
	OCDR	On-Chip Debug Register								227
$30 ($50)	SFIOR	ADTS2	ADTS1	ADTS0	–	ACME	PUD	PSR2	PSR10	57,88,134,201,221
$2F ($4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	110
$2E ($4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	113
$2D ($4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								114
$2C ($4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								114
$2B ($4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High Byte								114
$2A ($4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low Byte								114
$29 ($49)	OCR1BH	Timer/Counter1 – Output Compare Register B High Byte								114
$28 ($48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low Byte								114
$27 ($47)	ICR1H	Timer/Counter1 – Input Capture Register High Byte								114
$26 ($46)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte								114
$25 ($45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	128
$24 ($44)	TCNT2	Timer/Counter2 (8 Bits)								130
$23 ($43)	OCR2	Timer/Counter2 Output Compare Register								130
$22 ($42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	131
$21 ($41)	WDTCR	–	–	–	WDTOE	WDE	WDP2	WDP1	WDP0	43
$20[2] ($40)[2]	UBRRH	URSEL	–	–	–	UBRR[11:8]				167
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	166
$1F ($3F)	EEARH	–	–	–	–	–	–	–	EEAR8	19
$1E ($3E)	EEARL	EEPROM Address Register Low Byte								19
$1D ($3D)	EEDR	EEPROM Data Register								19
$1C ($3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	19
$1B ($3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	66
$1A ($3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	66
$19 ($39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	66
$18 ($38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	66
$17 ($37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	66
$16 ($36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	66
$15 ($35)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	67
$14 ($34)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	67
$13 ($33)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	67
$12 ($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	67
$11 ($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	67
$10 ($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	67
$0F ($2F)	SPDR	SPI Data Register								142
$0E ($2E)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	142
$0D ($2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	140
$0C ($2C)	UDR	USART I/O Data Register								163
$0B ($2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	164
$0A ($2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	165
$09 ($29)	UBRRL	USART Baud Rate Register Low Byte								167
$08 ($28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	202
$07 ($27)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	217
$06 ($26)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	219
$05 ($25)	ADCH	ADC Data Register High Byte								220
$04 ($24)	ADCL	ADC Data Register Low Byte								220
$03 ($23)	TWDR	Two-wire Serial Interface Data Register								182
$02 ($22)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	182

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$01 ($21)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	181
$00 ($20)	TWBR	Two-wire Serial Interface Bit Rate Register								180

Notes:
1. When the OCDEN Fuse is unprogrammed, the OSCCAL Register is always accessed on this address. Refer to the debugger specific documentation for details on how to use the OCDR Register.
2. Refer to the USART description for details on how to access UBRRH and UCSRC.
3. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
4. Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers $00 to $1F only.

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← $FF − Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← $00 − Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd − 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← $FF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
JMP	k	Direct Jump	PC ← k	None	3
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
CALL	k	Direct Subroutine Call	PC ← k	None	4
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd − Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd − Rr − C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd − K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1 / 2 / 3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-Chip Debug Only	None	N/A

Ordering Information

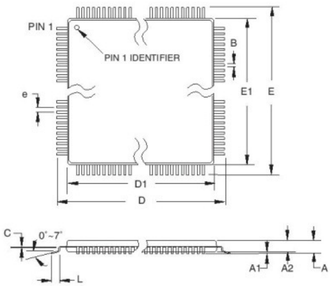
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
8	2.7V - 5.5V	ATmega16L-8AU[(1)] ATmega16L-8PU[(1)] ATmega16L-8MU[(1)]	44A 40P6 44M1	Industrial (-40°C to 85°C)
16	4.5V - 5.5V	ATmega16-16AU[(1)] ATmega16-16PU[(1)] ATmega16-16MU[(1)]	44A 40P6 44M1	Industrial (-40°C to 85°C)

Note: 1. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

Package Type	
44A	44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0 mm body, lead pitch 0.50 mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

Packaging Information

44A



COMMON DIMENSIONS
(Unit of Measure = mm)

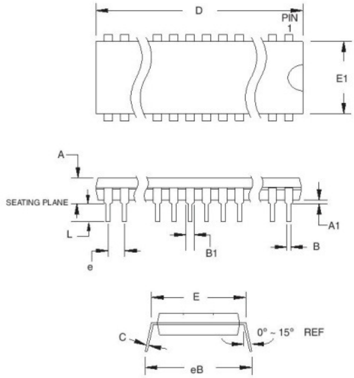
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e		0.80 TYP		

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	44A	B

40P6



COMMON DIMENSIONS
(Unit of Measure = mm)

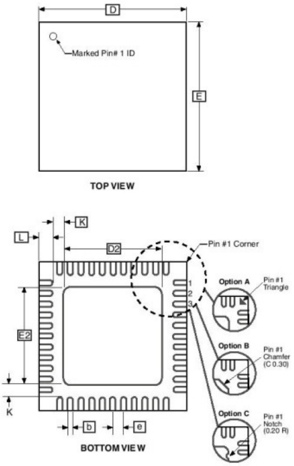
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

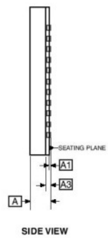
Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

44M1





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

9/26/08

Package Drawing Contact: packagedrawings@atmel.com	TITLE **44M1,** 44-pad, 7 x 7 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.20 mm Exposed Pad, Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (VQFN)	GPC	DRAWING NO.	REV.
		ZWS	44M1	H

Errata

The revision letter in this section refers to the revision of the ATmega16 device.

ATmega16(L) Rev. M

- **First Analog Comparator conversion may be delayed**
- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **IDCODE masks data from TDI input**
- **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request**

1. First Analog Comparator conversion may be delayed

If the device is powered by a slow rising V_{CC}, the first Analog Comparator conversion will take longer than expected on some devices.

Problem Fix/Workaround

When the device has been powered or reset, disable then enable theAnalog Comparator before the first conversion.

2. Interrupts may be lost when writing the timer registers in the asynchronous timer

The interrupt will be lost if a timer register that is synchronized to the asynchronous timer clock is written when the asynchronous Timer/Counter register(TCNTx) is 0x00.

Problem Fix / Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register(TCCRx), asynchronous Timer Counter Register(TCNTx), or asynchronous Output Compare Register(OCRx).

3. IDCODE masks data from TDI input

The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

Problem Fix / Workaround

- If ATmega16 is the only device in the scan chain, the problem is not visible.
- Select the Device ID Register of the ATmega16 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega16 while reading the Device ID Registers of preceding devices of the boundary scan chain.
- If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega16 must be the fist device in the chain.

4. Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.

Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

Problem Fix / Workaround

Always use OUT or SBI to set EERE in EECR.

ATmega16(L) Rev. L

- **First Analog Comparator conversion may be delayed**
- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **IDCODE masks data from TDI input**
- **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request**

1. First Analog Comparator conversion may be delayed

If the device is powered by a slow rising V_{CC}, the first Analog Comparator conversion will take longer than expected on some devices.

Problem Fix/Workaround

When the device has been powered or reset, disable then enable theAnalog Comparator before the first conversion.

2. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronized to the asynchronous timer clock is written when the asynchronous Timer/Counter register(TCNTx) is 0x00.

   Problem Fix / Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register(TCCRx), asynchronous Timer Counter Register(TCNTx), or asynchronous Output Compare Register(OCRx).

3. **IDCODE masks data from TDI input**

   The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

   Problem Fix / Workaround

   – If ATmega16 is the only device in the scan chain, the problem is not visible.
   – Select the Device ID Register of the ATmega16 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega16 while reading the Device ID Registers of preceding devices of the boundary scan chain.
   – If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega16 must be the fist device in the chain.

4. **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.**

   Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

   Problem Fix / Workaround

   Always use OUT or SBI to set EERE in EECR.

ATmega16(L) Rev. K

- **First Analog Comparator conversion may be delayed**
- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **IDCODE masks data from TDI input**
- **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request**

1. **First Analog Comparator conversion may be delayed**

   If the device is powered by a slow rising V_{CC}, the first Analog Comparator conversion will take longer than expected on some devices.

   Problem Fix/Workaround

   When the device has been powered or reset, disable then enable theAnalog Comparator before the first conversion.

2. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronized to the asynchronous timer clock is written when the asynchronous Timer/Counter register(TCNTx) is 0x00.

Problem Fix / Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register(TCCRx), asynchronous Timer Counter Register(TCNTx), or asynchronous Output Compare Register(OCRx).

3. **IDCODE masks data from TDI input**

The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

Problem Fix / Workaround

– If ATmega16 is the only device in the scan chain, the problem is not visible.

– Select the Device ID Register of the ATmega16 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega16 while reading the Device ID Registers of preceding devices of the boundary scan chain.

– If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega16 must be the fist device in the chain.

4. **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.**

Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

Problem Fix / Workaround

Always use OUT or SBI to set EERE in EECR.

ATmega16(L) Rev. J

- **First Analog Comparator conversion may be delayed**
- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **IDCODE masks data from TDI input**
- **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request**

1. **First Analog Comparator conversion may be delayed**

If the device is powered by a slow rising V_{CC}, the first Analog Comparator conversion will take longer than expected on some devices.

Problem Fix/Workaround

When the device has been powered or reset, disable then enable theAnalog Comparator before the first conversion.

2. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

The interrupt will be lost if a timer register that is synchronized to the asynchronous timer clock is written when the asynchronous Timer/Counter register(TCNTx) is 0x00.

Problem Fix / Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register(TCCRx), asynchronous Timer Counter Register(TCNTx), or asynchronous Output Compare Register(OCRx).

3. **IDCODE masks data from TDI input**

The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

Problem Fix / Workaround

– If ATmega16 is the only device in the scan chain, the problem is not visible.

– Select the Device ID Register of the ATmega16 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega16 while reading the Device ID Registers of preceding devices of the boundary scan chain.

– If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega16 must be the fist device in the chain.

4. **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.**

   Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

   Problem Fix / Workaround

   Always use OUT or SBI to set EERE in EECR.

ATmega16(L) Rev. I

- **First Analog Comparator conversion may be delayed**
- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **IDCODE masks data from TDI input**
- **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request**

1. **First Analog Comparator conversion may be delayed**

   If the device is powered by a slow rising V_{CC}, the first Analog Comparator conversion will take longer than expected on some devices.

   Problem Fix/Workaround

   When the device has been powered or reset, disable then enable theAnalog Comparator before the first conversion.

2. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronized to the asynchronous timer clock is written when the asynchronous Timer/Counter register(TCNTx) is 0x00.

   Problem Fix / Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register(TCCRx), asynchronous Timer Counter Register(TCNTx), or asynchronous Output Compare Register(OCRx).

3. **IDCODE masks data from TDI input**

   The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

   Problem Fix / Workaround

   – If ATmega16 is the only device in the scan chain, the problem is not visible.

   – Select the Device ID Register of the ATmega16 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega16 while reading the Device ID Registers of preceding devices of the boundary scan chain.

   – If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega16 must be the fist device in the chain.

4. **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.**

   Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

   Problem Fix / Workaround

   Always use OUT or SBI to set EERE in EECR.

ATmega16(L) Rev. H

- **First Analog Comparator conversion may be delayed**
- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **IDCODE masks data from TDI input**
- **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request**

1. **First Analog Comparator conversion may be delayed**

   If the device is powered by a slow rising V_{CC}, the first Analog Comparator conversion will take longer than expected on some devices.

   Problem Fix/Workaround

   When the device has been powered or reset, disable then enable theAnalog Comparator before the first conversion.

2. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronized to the asynchronous timer clock is written when the asynchronous Timer/Counter register(TCNTx) is 0x00.

   Problem Fix / Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register(TCCRx), asynchronous Timer Counter Register(TCNTx), or asynchronous Output Compare Register(OCRx).

3. **IDCODE masks data from TDI input**

   The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

   Problem Fix / Workaround

   – If ATmega16 is the only device in the scan chain, the problem is not visible.

   – Select the Device ID Register of the ATmega16 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega16 while reading the Device ID Registers of preceding devices of the boundary scan chain.

   – If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega16 must be the fist device in the chain.

4. **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.**

   Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

   Problem Fix / Workaround

   Always use OUT or SBI to set EERE in EECR.

Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

Rev. 2466T-07/10

1. Corrected use of comma in formula Rp in Table 120, "Two-wire Serial Bus Requirements," on page 294.
2. Updated document according to Atmel's Technical Terminology
3. Note 6 and Note 7 under Table 120, "Two-wire Serial Bus Requirements," on page 294 have been removed.

Rev. 2466S-05/09

1. Updated "Errata" on page 340.
2. Updated the last page with Atmel's new adresses.

Rev. 2466R-06/08

1. Added "Not recommended for new designs" note in Figure on page 1.

Rev. 2466Q-05/08

1. Updated "Fast PWM Mode" on page 77 in "8-bit Timer/Counter0 with PWM" on page 71:
   – Removed the last section describing how to achieve a frequency with 50% duty cycle waveform output in fast PWM mode.
2. Removed note from Feature list in "Analog to Digital Converter" on page 204.
3. Removed note from Table 84 on page 218.
4. Updated "Ordering Information" on page 336:
   - Commercial ordering codes removed.
   - Non Pb-free package option removed.

Rev. 2466P-08/07

1. Updated "Features" on page 1.
2. Added "Data Retention" on page 6.
3. Updated "Errata" on page 340.
4. Updated "Slave Mode" on page 140.

Rev. 2466O-03/07

1. Updated "Calibrated Internal RC Oscillator" on page 29.
2. Updated C code example in "USART Initialization" on page 149.
3. Updated "ATmega16 Boundary-scan Order" on page 241.
4. Removed "premilinary" from "ADC Characteristics" on page 297.
5. Updated from V to mV in "I/O Pin Input Hysteresis vs. V_{CC}" on page 317.
6. Updated from V to mV in "Reset Input Pin Hysteresis vs. V_{CC}" on page 318.

Rev. 2466N-10/06

1. Updated "Timer/Counter Oscillator" on page 31.
2. Updated "Fast PWM Mode" on page 102.
3. Updated Table 38 on page 83, Table 40 on page 84, Table 45 on page 111, Table 47 on page 112, Table 50 on page 128 and Table 52 on page 129.
4. Updated C code example in "USART Initialization" on page 149.
5. Updated "Errata" on page 340.

Rev. 2466M-04/06

1. Updated typos.
2. Updated "Serial Peripheral Interface – SPI" on page 135.
3. Updated Table 86 on page 221, Table 116 on page 276 ,Table 121 on page 295 and Table 122 on page 297.

Rev. 2466L-06/05

1. Updated note in "Bit Rate Generator Unit" on page 178.
2. Updated values for V_{INT} in "ADC Characteristics" on page 297.
3. Updated "Serial Programming Instruction set" on page 276.
4. Updated USART init C-code example in "USART" on page 144.

Rev. 2466K-04/05

1. Updated "Ordering Information" on page 336.
2. MLF-package alternative changed to "Quad Flat No-Lead/Micro Lead Frame Package QFN/MLF".
3. Updated "Electrical Characteristics" on page 291.

Rev. 2466J-10/04

1. Updated "Ordering Information" on page 336.

Rev. 2466I-10/04

1. Removed references to analog ground.
2. Updated Table 7 on page 28, Table 15 on page 38, Table 16 on page 42, Table 81 on page 209, Table 116 on page 276, and Table 119 on page 293.
3. Updated "Pinout ATmega16" on page 2.
4. Updated features in "Analog to Digital Converter" on page 204.
5. Updated "Version" on page 229.
6. Updated "Calibration Byte" on page 261.
7. Added "Page Size" on page 262.

Rev. 2466H-12/03

1. Updated "Calibrated Internal RC Oscillator" on page 29.

Rev. 2466G-10/03

1. Removed "Preliminary" from the datasheet.
2. Changed ICP to ICP1 in the datasheet.
3. Updated "JTAG Interface and On-chip Debug System" on page 36.
4. Updated assembly and C code examples in "Watchdog Timer Control Register – WDTCR" on page 43.
5. Updated Figure 46 on page 103.
6. Updated Table 15 on page 38, Table 82 on page 217 and Table 115 on page 276.
7. Updated "Test Access Port – TAP" on page 222 regarding JTAGEN.
8. Updated description for the JTD bit on page 231.
9. Added note 2 to Figure 126 on page 252.
10. Added a note regarding JTAGEN fuse to Table 105 on page 260.
11. Updated Absolute Maximum Ratings* and DC Characteristics in "Electrical Characteristics" on page 291.
12. Updated "ATmega16 Typical Characteristics" on page 299.
13. Fixed typo for 16 MHz QFN/MLF package in "Ordering Information" on page 336.
14. Added a proposal for solving problems regarding the JTAG instruction IDCODE in "Errata" on page 340.

Rev. 2466F-02/03

1. Added note about masking out unused bits when reading the Program Counter in "Stack Pointer" on page 12.
2. Added Chip Erase as a first step in "Programming the Flash" on page 288 and "Programming the EEPROM" on page 289.
3. Added the section "Unconnected pins" on page 55.
4. Added tips on how to disable the OCD system in "On-chip Debug System" on page 34.
5. Removed reference to the "Multi-purpose Oscillator" application note and "32 kHz Crystal Oscillator" application note, which do not exist.
6. Added information about PWM symmetry for Timer0 and Timer2.
7. Added note in "Filling the Temporary Buffer (Page Loading)" on page 253 about writing to the EEPROM during an SPM Page Load.
8. Removed ADHSM completely.

9. **Added Table 73, "TWI Bit Rate Prescaler," on page 182 to describe the TWPS bits in the "TWI Status Register – TWSR" on page 181.**

10. **Added section "Default Clock Source" on page 25.**

11. **Added note about frequency variation when using an external clock. Note added in "External Clock" on page 31. An extra row and a note added in Table 118 on page 293.**

12. **Various minor TWI corrections.**

13. **Added "Power Consumption" data in "Features" on page 1.**

14. **Added section "EEPROM Write During Power-down Sleep Mode" on page 22.**

15. **Added note about Differential Mode with Auto Triggering in "Prescaling and Conversion Timing" on page 207.**

16. **Added updated "Packaging Information" on page 337.**

Rev. 2466E-10/02

1. **Updated "DC Characteristics" on page 291.**

Rev. 2466D-09/02

1. **Changed all Flash write/erase cycles from 1,000 to 10,000.**

2. **Updated the following tables: Table 4 on page 26, Table 15 on page 38, Table 42 on page 85, Table 45 on page 111, Table 46 on page 111, Table 59 on page 143, Table 67 on page 167, Table 90 on page 235, Table 102 on page 258, "DC Characteristics" on page 291, Table 119 on page 293, Table 121 on page 295, and Table 122 on page 297.**

3. **Updated "Errata" on page 340.**

Rev. 2466C-03/02

1. **Updated typical EEPROM programming time, Table 1 on page 20.**

2. **Updated typical start-up time in the following tables:**
   Table 3 on page 25, Table 5 on page 27, Table 6 on page 28, Table 8 on page 29, Table 9 on page 29, and Table 10 on page 29.

3. **Updated Table 17 on page 43 with typical WDT Time-out.**

4. **Added Some Preliminary Test Limits and Characterization Data.**
   Removed some of the TBD's in the following tables and pages:
   Table 15 on page 38, Table 16 on page 42, Table 116 on page 272 (table removed in document review #D), "Electrical Characteristics" on page 291, Table 119 on page 293, Table 121 on page 295, and Table 122 on page 297.

5. **Updated TWI Chapter.**
   Added the note at the end of the "Bit Rate Generator Unit" on page 178.

6. **Corrected description of ADSC bit in "ADC Control and Status Register A – ADCSRA" on page 219.**

7. **Improved description on how to do a polarity check of the ADC doff results in "ADC Conversion Result" on page 216.**

8. **Added JTAG version number for rev. H in Table 87 on page 229.**

9. **Added not regarding OCDEN Fuse below Table 105 on page 260.**

10. **Updated Programming Figures:**

    Figure 127 on page 262 and Figure 136 on page 273 are updated to also reflect that AVCC must be connected during Programming mode. Figure 131 on page 269 added to illustrate how to program the fuses.

11. **Added a note regarding usage of the "PROG_PAGELOAD ($6)" on page 280 and "PROG_PAGEREAD ($7)" on page 280.**

12. **Removed alternative algortihm for leaving JTAG Programming mode.**

    See "Leaving Programming Mode" on page 288.

13. **Added Calibrated RC Oscillator characterization curves in section "ATmega16 Typical Characteristics" on page 299.**

14. **Corrected ordering code for QFN/MLF package (16MHz) in "Ordering Information" on page 336.**

15. **Corrected Table 90, "Scan Signals for the Oscillators(1)(2)(3)," on page 235.**

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
avr@atmel.com

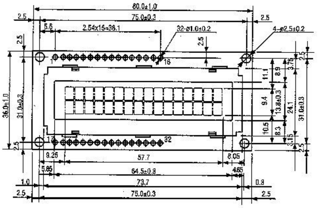
Sales Contact
www.atmel.com/contacts

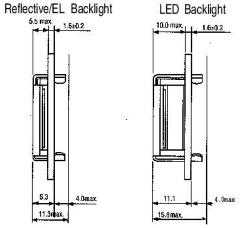
Literature Requests
www.atmel.com/literature

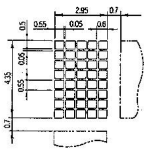
2466TS–AVR–07/10

Lampiran LCD Karakter

L1682 (2x16) Unit: mm General Tolerance f0.5 mm



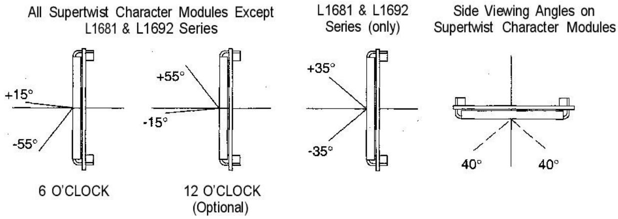




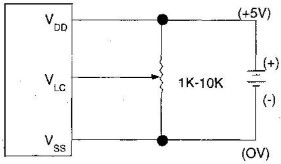
*LED Powered through pins 15 & 16 or 31 & 32

PIN FUNCTIONS			
No.	**No.**	**Name**	**Function**
1	17	V_{SS}	GND
2	18	V_{DD}	Power supply voltage + 5 V
3	19	V_{LC}	Liquid crystal driving voltage
4	20	RS	L: Instruction code input. H: Data input
5	21	R/W	L: Data write from MPU to LCM. H: Data read from LCM to MPU
6	22	E	Enable
7	23	DB0	Data bus line
8	24	DB1	Data bus line
9	25	DB2	Data bus line
10	26	DB3	Data bus line
11	27	DB4	Data bus line
12	28	DB5	Data bus line
13	29	DB6	Data bus line
14	30	DB7	Data bus line
15	31	V_A*	Anode
16	32	V_K*	Cathode

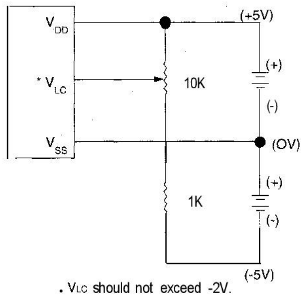
Optimum Viewing Angle / Contrast Adjustment Circuit



Standard STN & 12022



Wide Temperature STN



* V_{LC} should not exceed -2V.

- The above schematic applies to all **Seiko Instruments** standard temperature supertwist character modules except L2022. A variable or fixed resistor must be used on any LCD module as it appears in the above schematic.
- A variable resistor is advisable, especially for stationary equipment. The variable resistor allows the user to adjust the voltage, to get maximum contrast in relationship to whatever angle the user is viewing the LCD (within the optimum viewing range). A variable also allows the user to adjust the voltage for any temperature fluctuations between 0" and 50°C.
- A fixed resistor limits the LCD to a finite voltage and therefore a very limited viewing angle. Fixed resistors should be used in those applications where the display can be adjusted to the particular user (i.e., hand-held products).

- The above schematic applies to all **Seiko Instruments** supertwist character modules with Wide Temperature Fluid. A variable or fixed resistor must be used on any LCD module as it appears in the above schematic.
- A variable resistor is advisable, especially for stationary equipment. The variable resistor allows the user to adjust the voltage, to get maximum contrast in relationship to whatever angle the user is viewing the LCD (within the optimum viewing range). A variable also allows the user to adjust the voltage for any temperature fluctuations between -20° and 70%.
- A fixed resistor limits the LCD to a finite voltage and therefore a very limited viewing angle. Fixed resistors should be used in those applications where the display can be adjusted to the particular user (i.e., hand-held products).

OPERATING INSTRUCTIONS

INTRODUCTION

Seiko Instruments intelligent dot matrix liquid crystal display modules have on-board controller and LSI drivers, which display alpha numerics, Japanese KATA KANA characters and a wide variety of other symbols in either 5 x 7 dot matrix.

The internal operation in the KS0006 controller chip is determined by signals sent from the MPU. The signals include: 1) Register select RS input consisting of instruction register (IR) when RS = 0 and data register (DR) when RS = 1; 2) Read/write (R/W); 3) Data bus (DB7~ DBO); and 4) Enable strobe (E) depending on the MPU or through an external parallel I/O port. Details on instructions data entry, execution times, etc. are explained in the following sections.

READ AND WRITE TIMING DIAGRAMS AND TABLES

The following timing characteristics are applicable for all of Seiko's LCD dot matrix character modules.

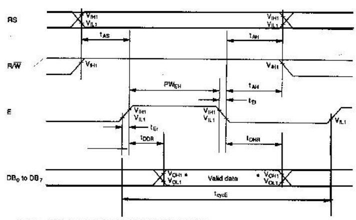
READ TIMING CHARACTERISTICS
V_{DD}=5.0V±5%, V_{SS}=OV, T_a=0°C TO 50°C

item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		$t_{CYC}E$	500	—	ns
Enable pulse width	High Level	PW_{EH}	230	—	ns
Enable rise and fall time		t_{ER}, t_{EF}	—	20	ns
Setup time	RS,R/W—E	t_{AS}	140	—	ns
Address hold time		t_{AH}	10	—	ns
Data delay time		t_{DDR}	—	160	ns
Data hold time		t_H	5	—	ns

WRITE TIMING CHARACTERISTICS
V_{DD}=5.0V±5%, V_{SS}=OV, T_a=0°C TO 50°C

Item		Symbol	Standard		Unit
			Min.	Max.	
Enable cycle time		$t_{CYC}E$	500	—	ns
Enable pulse width	High Level	PW_{EH}	230	—	ns
Enable rise and fall time		t_{ER}, t_{EF}	—	20	ns
Setup time	RS,R/W-E	t_{AS}	140	—	ns.
Address hold time		t_{AH}	10	—	ns
Data delay time		t_{DDR}	80	—	ns
Data hold time		t_H	10	—	ns

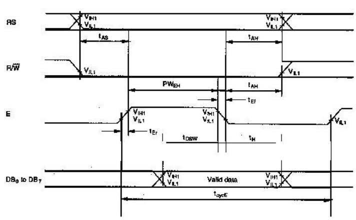
READ OPERATION



Note: • VOLI is assumed to be 0.8 Vat 2 MHz operation.

DATA READ FROM MODULE TO MPU

WRITE OPERATION



DATA WRITE FROM MPU TO MODULE

INSTRUCTION CODES

Instruction	Set		Instruction Code								Description	Execution Time (when f_{cp} or f_{osc} is 250 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display memory and returns the cursor to the home position (Address 0).	82 μs - 1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0) shifted to the original position. DD RAM contents remain unchanged.	40 μs ~ 1.6ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies to or not to shift the display. These operations write and read.	40 μs ~ 1.64ms
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	(D) is display ON/OFF control; memory remains unchanged in OFF condition. (C) cursor ON/OFF (B) blinking cursor.	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N), and character font(F).	40 μs
Set CG RAM Address	0	0	0	1	A_{CG}						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set DD RAM Address	0	0	1	A_{DD}							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents.	1 μs
Write Data to CG or to DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs

* Doesn't matter

DD RAM: Display data RAM
CG RAM: Character generator RAM
A_{CG}: CG RAM address
A_{DD}: DD RAM address corresponds to cursor address
AC: Address counter used for both DD RAM and CG RAM address

I/D = 1: increment
I/D = 0: Decrement
S=1: Display shift
S=0: No display shift
D-l: Display ON
D=0: Display OFF

C=1: Cursor ON
c=0: Cursor OFF
B=l: Blink ON
B=O: Blink OFF
S/C = 1: Display shift
S/C = 0: Cursor movement
BF=1: Internal operation in progress
BF=0: instruction can be accepted

R/L=1: Right shift
R/L = 0: Left shift
DL=l: 6 bits
DL=O: 4 bits
N=1: 2 lines (L1671)
F=0: 5 x 7 dot matrix

Execution times in the above table indicate the minimum values when operating frequency is 250 kHz.

When f_{osc} is 270 kHz: 40μs x 250/250 = 37μs

INSTRUCTION CODE EXPLANATIONS

The two registers 1) Instruction Register (IR) and the 2) Data Register (DR) in the KS0066 controller chip are directly controlled by the MPU. Control information is temporarily stored in these registers prior to internal operation start. This allows interface to various types of MPUs which operate at different speeds from that of the KS0066, and allows interface from peripheral control ICs. Internal operations of the KS0066 are determined from the signals sent from the MPU. These signals, including register selection signals (RS), Read/Write (R/W) and data bus signals (DBO - DB7) are polled instructions.

REGISTER SELECTION

RS	R/W	Operation
0	0	IR selection, IR write. Internal operation: Display clear
0	1	**Busy** flag (DB7) and address counter (DBO to DB6) read
1	0	DR selection, DR write. Internal operation: DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation: DD RAM or CG RAM to DR

ADDRESS COUNTER (AC)

The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DBO to DB6; refer to above "Register Selection Table" when RS = 0 and R/W= 1.

CLEAR DISPLAY

	RS	R/W	DB7							DBO
Code	0	0	0	0	0	0	0	0	0	1

Clear all display memory and return the cursor to the home position. In other words, the cursor returns to the first character block on the first line on all 1, 2, and 4 line character modules except L4044. If the above is entered on E2 (the second controller for lines 3 and 4), the cursor will return to the first character on the third line.

CURSOR HOME

	RS	R/W	DB7							DBO
Code	0	0	0	0	0	0	0	0	1	*

*Doesn't matter

Returns cursor to home position. First line first character blocks on all 1, 2 and 4 line display; except L4044 refer "clear display": (Address 0; A,, "80"). The contents of DD RAM remain unchanged.

RESTRICTIONS ON EXECUTION OF DISPLAY CLEAR AND CURSOR HOME INSTRUCTIONS

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction).	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{OSC}$* second after the first execution. • L4052: f_{OSC} = 250 kHz • The other modules: f_{OSC} = 270 kHz *f_{OSC}: Oscillation frequency
When 23_H, 27_H, 63_H, or 67_H is used as a DD RAM address to execute Cursor Home instruction.	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

Entry Mode Set

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	0	1	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by one block when writing or reading a character code from DD RAM or CG RAM. The cursor automatically moves to the right when incremented by one or to the left if decremented by one.

S: Shifts the entire display to either the right or left when S = 1 (high). When S = 1 and I/D = 1 the display shifts one position to the left. When S = 1 and I/D = 0 the display shifts one position to the right. This right or left shift occurs after each data write to DD RAM. Display is not shifted when reading from DD RAM. Display is not shifted when S = 0.

Display and Cursor ON/OFF Control

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	1	D	C	B

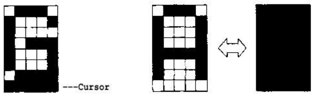
D: Display is turned ON when D = 1 and OFF when D = 0. When display is OFF, display data in DD RAM remains unchanged. Information comes back immediately when D = 1 is entered.

C: Cursor is displayed when C = 1 and not displayed when C = 0. If the cursor disappears, function of I/D etc. does not change during display data write. In a 5 x 7 dot matrix there is an eighth line which functions as the cursor.

B: When B = 1, the character at the cursor position starts blinking. When B = 0 the cursor does not blink. The blink is done by stiching between the all black dot matrix and displayed character at 0.4 second intervals. The cursor and the blink can be set at the same time (fosc = 250 kHz).

5 X 7 DOT MATRIX

C = 1 (cursor display) B = 1 (blinking)



Cursor or Display Shift

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* Doesn't Matter

Cursor/Display Shift moves the cursor or shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. In case of a 2-line display, the cursor is shifted from character block 40 of line 1 to character block 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. In case of a 4-line display, the cursor does not move continuously from line 2 to line 3. The cursor is shifted from character block 40 of line 3 to character block 1 of line 4. Displays of lines 3 and 4 are shifted at the same time. The display pattern of line 2 or 4 is not shifted to line 1 or 3.

SIC	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one)
0	1	The cursor position is shifted to the right (the AC increments one)
1	0	The entire display is shifted to the left with the cursor
1	1	The entire display is shifted to the right with the cursor

FUNCTION SET

	RS	R/W	DB7							DBO
Code	0	0	0	0	1	DL	N	F	*	*

* Doesn't Matter

Function Set sets the interface data length, the number of display lines and the character font.

DL: Interface data length

When DL = 1, the data length is set at 8 bits (DB7 to DBO).

When DL = 0, the data length is set at 4 bits (DB7 to DB4).

The upper 4 bits are transferred first, then the lower 4 bits follow.

N: Number of display lines

F: Sets character font

1	0	2	5 x 7 dot matrix	l/16	L1671, L1681, L1672, L1682 L1692, L1634, L2032, L2022 L2034, L2462, L4052, L4044

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

CG RAM ADDRESS SET

	RS	R/W	DB7							DBO
Code	0	0	0	1	A	A	A	A	A	A

← Upper bit Lower bit →

CG RAM addresses, expressed as binary AAAAAA, are set to the AC. Then data in CG RAM is written from or read to the MPU.

DD RAM ADDRESS SET

	RS	R/W	DB7							DBO
Code	0	0	0	1	A	A	A	A	A	A

← Upper bit Lower bit →

DD RAM addresses expressed as binary AAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU.

BUSY FLAG/ADDRESS READ

	RS	R/W	DB7							DBO
Code	0	0	0	1	A	A	A	A	A	A

← Upper bit Lower bit →

The BF signal can be read to verify if the controller is indicating that the module is working on a current instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

DATA WRITE TO CG RAM OR DD RAM

	RS	R/W	DB7							DBO
Code	1	0	D	D	D	.D	D	D	D	D

← Upper bit Lower bit →

Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction or the DD RAM Address Set instruction before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

DATA READ FROM CG RAM OR DD RAM

	RS	R/W	DB7							DBO
Code		1	1	D	D	D	D	D	D	D	D

← Upper bit Lower bit →

Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction or the DD RAM Address Set instruction before this instruction selects either RAM. In addition, either instruction is executed immediately before this instruction. If no Address Set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.

After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note: The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

5 x 7 + CURSOR

Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data), (5 x 7 dot matrix).

Character code (DD RAM data) 7 6 5 4 3 2 1 0 ←Upper bit Lower bit→	CG RAM address 5 4 3 ←Upper bit	CG RAM address 2 1 0 Lower bit→	Character pattern (CG RAM data) 7 6 5 ←Upper bit	Character pattern (CG RAM data) 4 3 2 1 0 Lower bit→	
0 0 0 0 * 0 0 0	0 0 0	0 0 0	* * *	1 1 1 1 0	Example of character pattern (R)
		0 0 1	↑	1 0 0 0 1	
		0 1 0		1 0 0 0 1	
		0 1 1		1 1 1 1 0	
		1 0 0		1 0 1 0 0	
		1 0 1		1 0 0 1 0	
		1 1 0	↓	1 0 0 0 1	
		1 1 1	* * *	0 0 0 0 0	← Cursor position
0 0 0 0 * 0 0 1	0 0 1	0 0 0	* * *	1 0 0 0 1	Example of character pattern (Y)
		0 0 1	↑	0 1 0 1 0	
		0 1 0		1 1 1 1 1	
		0 1 1		0 0 1 0 0	
		1 0 0		1 1 1 1 1	
		1 0 1		0 0 1 0 0	
		1 1 0	↓	0 0 1 0 0	
		1 1 1	* * *	0 0 0 0 0	
0 0 0 0 * 1 1 1	1 1 1	0 0 0	* * *		
		0 0 1	↑		
		1 0 0			
		1 0 1			
		1 1 0	↓		
		1 1 1	* * *		

NOTES:
- In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.
- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).
- CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is charged to 1, one bit lights, regardless of the cursor.
- The character pattern column position corresponds to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.
- When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

PROGRAMMING THE CHARACTER GENERATOR RAM (CG RAM)

The character generator RAM (CG RAM) allows the user to create up to eight custom 5 x 7 characters + cursor (5 x 8). Once programmed, the custom characters or symbols are accessed exactly as if they were in ROM. However since the RAM is a volatile memory, power must be continually maintained. Otherwise, the custom characters/symbols must be programmed into non-volatile external ROM and sent to the display after each display initialization. All dots in the 5 x 8 dot matrix can be programmed, which includes the cursor position.

The modules RAM are divided into two parts: data display RAM (DD RAM) and custom character generator RAM (CG RAM). This is not to be confused programming the custom character generator RAM with the 192 character generator ROM. The CG RAM is located between hex 40 and 7F and is contiguous. Locations 40 thru 47 hold the first custom character (5 x 8), 48 thru 4F hold the second custom character, 50 thru 57 hold the third CG, and so forth to 78 thru 7F for the eighth CG character/symbol.

If during initialization the display was programmed to automatically increment, then only the single initial address, 40, need be sent. Consecutive row data will automatically appear at 41, 42, etc. until the completed character is formed. All eight custom CG characters can be programmed in 64 consecutive "writes" after sending the single initial 40 address.

The CG RAM is 8 bits wide, although only the right-most 5-bits are used for a custom CG character row. The left-most dot of programming the CG RAM character corresponds to D4 in the most significant nibble (XXXD4) of the data bus code, with the remaining 4 dots in the row corresponding to the least significant nibble (D3 thru DO), DO being the right-most dot. Thus, hex 1 F equals all dots on and hex 00 equals all dots off. Examples include hex 15 (10101) equal to 3 dots on the hex OA (01010) equal 2 dots on. In each case the key 5-bits of the 8-bit code program one row of a custom CG character. When all 7 or 8 rows are programmed, the character is complete. A graphic example is shown below:

RS	R/W	Data	Display	Description
0	0	40	—	addresses 1st row, 1st CG character
1	0	11	* *	result of 11, 1 st row
1	0	OA	**	result of OA, 2nd row
1	0	1F	*****	result of 1 F, 3rd row
1	0	04	*	result of 04, 4th row
1	0	1F	*****	result of 1 F, 5th row
1	0	04	*	result of 04, 6th row
1	0	04	*	result of 04, 7th row
1	0	00	—	result of 00, 8th row (cursor position)
1	0	15	***	1st row, 2nd CG character. **Note:** Addressing not now required; hex 48 is next in the sequence.

2) L1672-Series (16 characters x 2 lines)
L1682-Series
L1692-Series

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
Line 2	CO	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF

Order this document by LM339/D

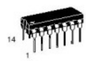
MOTOROLA

Quad Single Supply Comparators

LM339, LM339A, LM239, LM239A, LM2901, M2901V, MC3302

These comparators are designed for use in level detection, low–level sensing and memory applications in consumer automotive and industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ±5.0 nA (Typ)
- Low Input Offset Voltage: ±1.0 mV (Typ) LM139A Series
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- ESD Clamps on the Inputs Increase Reliability without Affecting Device Operation



N, P SUFFIX
PLASTIC PACKAGE
CASE 646

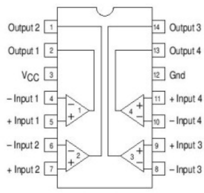
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage LM239, A/LM339A/LM2901, V MC3302	V_{CC}	 +36 or ±18 +30 or ±15	Vdc
Input Differential Voltage Range LM239, A/LM339A/LM2901, V MC3302	V_{IDR}	 36 30	Vdc
Input Common Mode Voltage Range	V_{ICMR}	–0.3 to V_{CC}	Vdc
Output Short Circuit to Ground (Note 1)	I_{SC}	Continuous	
Power Dissipation @ T_A = 25°C Plastic Package Derate above 25°C	P_D	 1.0 8.0	 W mW/°C
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range LM239, A MC3302 LM2901 LM2901V LM339, A	T_A	 –25 to +85 –40 to +85 –40 to +105 –40 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

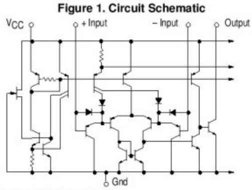
NOTE: 1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.

PIN CONNECTIONS



(Top View)

Figure 1. Circuit Schematic



NOTE: Diagram shown is for 1 comparator.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM239D,AD LM239N,AN	T_A = 25° to +85°C	SO–14 Plastic DIP
LM339D, AD LM339N, AN	T_A = 0° to +70°C	SO–14 Plastic DIP
LM2901D LM2901N	T_A = –40° to +105°C	SO–14 Plastic DIP
LM2901VD LM2901VN	T_A = –40° to +125°C	SO–14 Plastic DIP
MC3302P	T_A = –40° to +85°C	Plastic DIP

 Rev 2

LM339, LM339A, LM239, LM239A, LM2901, M2901V, MC3302

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = +25°C, unless otherwise noted)

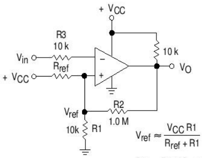
Characteristic	Symbol	LM239A/339A			LM239/339			LM2901/2901V			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	–	±1.0	±2.0	–	±2.0	±5.0	–	±2.0	±7.0	–	±3.0	±20	mVdc
Input Bias Current (Notes 4, 5) (Output in Analog Range)	I_{IB}	–	25	250	–	25	250	–	25	250	–	25	500	nA
Input Offset Current (Note 4)	I_{IO}	–	±5.0	±50	–	±5.0	±50	–	±5.0	±50	–	±3.0	±100	nA
Input Common Mode Voltage Range	V_{ICMR}	0	–	V_{CC} −1.5	0	–	V_{CC} −1.5	0	–	V_{CC} −1.5	0	–	V_{CC} −1.5	V
Supply Current	I_{CC}													mA
$R_L = \infty$ (For All Comparators)		–	0.8	2.0	–	0.8	2.0	–	0.8	2.0	–	0.8	2.0	
$R_L = \infty$, V_{CC} = 30 Vdc		–	1.0	2.5	–	1.0	2.5	–	1.0	2.5	–	1.0	2.5	
Voltage Gain $R_L \geq$ 15 kΩ, V_{CC} = 15 Vdc	A_{VOL}	50	200	–	50	200	–	25	100	–	25	100	–	V/mV
Large Signal Response Time V_I = TTL Logic Swing, V_{ref} = 1.4 Vdc, V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	–	–	300	–	–	300	–	–	300	–	–	300	–	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	–	–	1.3	–	–	1.3	–	–	1.3	–	–	1.3	–	µs
Output Sink Current $V_I(-) \geq$ +1.0 Vdc, $V_I(+)$ = 0, $V_O \leq$ 1.5 Vdc	I_{Sink}	6.0	16	–	6.0	16	–	6.0	16	–	6.0	16	–	mA
Saturation Voltage $V_I(-) \geq$ +1.0 Vdc, $V_I(+)$ = 0, $I_{sink} \leq$ 4.0 mA	V_{sat}	–	130	400	–	130	400	–	130	400	–	130	500	mV
Output Leakage Current $V_I(+) \geq$ +1.0 Vdc, $V_I(-)$ = 0, V_O = +5.0 Vdc	I_{OL}	–	0.1	–	–	0.1	–	–	0.1	–	–	0.1	–	nA

PERFORMANCE CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = T_{low} to T_{high} [Note 3])

Characteristic	Symbol	LM239A/339A			LM239/339			LM2901/2901V			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	–	–	±4.0	–	–	±9.0	–	–	±15	–	–	±40	mVdc
Input Bias Current (Notes 4, 5) (Output in Analog Range)	I_{IB}	–	–	400	–	–	400	–	–	500	–	–	1000	nA
Input Offset Current (Note 4)	I_{IO}	–	–	±150	–	–	±150	–	–	±200	–	–	±300	nA
Input Common Mode Voltage Range	V_{ICMR}	0	–	V_{CC} −2.0	0	–	V_{CC} −2.0	0	–	V_{CC} −2.0	0	–	V_{CC} −2.0	V
Saturation Voltage $V_I(-) \geq$ +1.0 Vdc, $V_I(+)$ = 0, $I_{sink} \leq$ 4.0 mA	V_{sat}	–	–	700	–	–	700	–	–	700	–	–	700	mV
Output Leakage Current $V_I(+) \geq$ +1.0 Vdc, $V_I(-)$ = 0, V_O = 30 Vdc	I_{OL}	–	–	1.0	–	–	1.0	–	–	1.0	–	–	1.0	µA
Differential Input Voltage All $V_I \geq$ 0 Vdc	V_{ID}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	Vdc

NOTES: 3. (LM239/239A) T_{low} = −25°C, T_{high} = +85°
(LM339/339A) T_{low} = 0°C, T_{high} = +70°C
(MC3302) T_{low} = −40°C, T_{high} = +85°C
(LM2901) T_{low} = −40°C, T_{high} = +105°
(LM2901V) T_{low} = −40°C, T_{high} = +125°C
4. At the output switch point, $V_O \simeq$ 1.4 Vdc, $R_S \leq$ 100 Ω 5.0 Vdc $\leq V_{CC} \leq$ 30 Vdc, with the inputs over the full common mode range (0 Vdc to V_{CC} −1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

Figure 2. Inverting Comparator with Hystersis



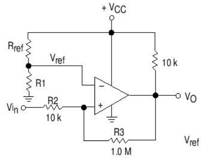
$$V_{ref} \approx \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R3 \simeq R1 \,//\, R_{ref} \,//\, R2$$

$$V_H = \frac{R1 \,//\, R_{ref}}{R1 \,//\, R_{ref} + R2}\,[V_{O(max)} - V_{O(min)}]$$

$$R2 \gg Rref \,//\, R1$$

Figure 3. Noninverting Comparator with Hysteresis



$$V_{ref} = \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R2 \approx R1 \,//\, R_{ref}$$

Amount of Hysteresis V_H

$$V_H = \frac{R2}{R2 + R3}\,[(V_{O(max)} - V_{O(min)}]$$

Typical Characteristics

(V_{CC} = 15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

Figure 4. Normalized Input Offset Voltage

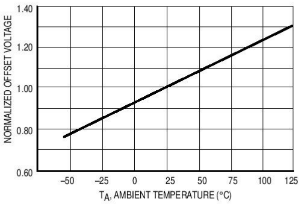


Figure 5. Input Bias Current

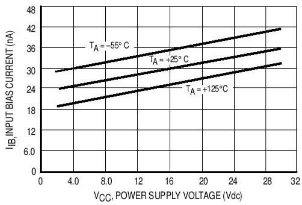


Figure 6. Output Sink Current versus Output Saturation Voltage

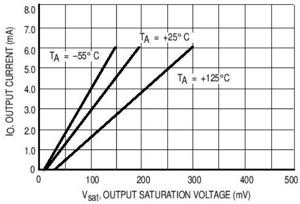
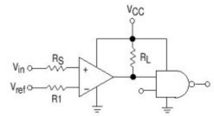


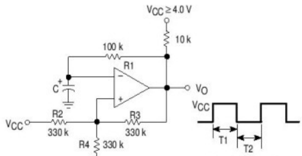
Figure 7. Driving Logic



R_S = Source Resistance
$R1 \approx R_S$

Logic	Device	V_{CC} (V)	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

Figure 8. Squarewave Oscillator



$T1 = T2 = 0.69\ RC$

$f \approx \frac{7.2}{C(\mu F)}$

$R2 = R3 = R4$

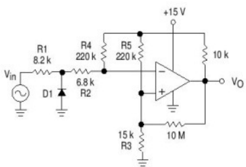
$R1 \approx R2 // R3 // R4$

APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than −300 mV should not be used.

Figure 9. Zero Crossing Detector (Single Supply)



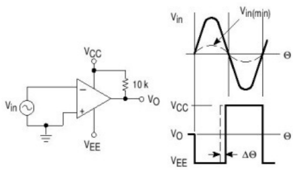
D1 prevents input from going negative by more than 0.6 V.

$R1 + R2 = R3$

$R3 \leq \frac{R5}{10}$ for small error in zero crossing

Figure 10. Zero Crossing Detector (Split Supplies)

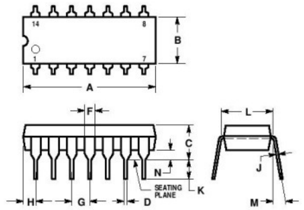
$V_{in(min)} \approx 0.4$ V peak for 1% phase distortion ($\Delta\Theta$).



LM339, LM339A, LM239, LM239A, LM2901, M2901V, MC3302

OUTLINE DIMENSIONS

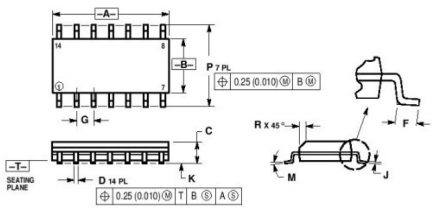
N, P SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
(SO–14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

LAMPIRAN 5
DATA SHEET SENSOR OPTOCOUPLER

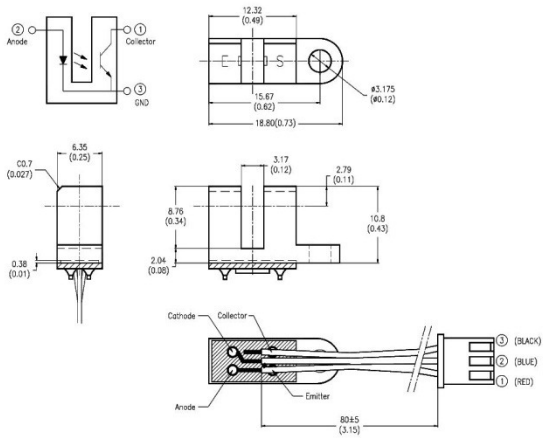
FEATURES

* NON-CONTCACT SWITCHING.
* 3 PIN CONNECTOR.

APPLICATION

* SCANNER,PRINTER.

PACKAGE DIMENSIONS



NOTES:

1. All dimensions are in millimeters (inches).
2. Tolerance is ±0.25mm(.010") unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS AT T_A=25℃

PARAMETER	SYMBOL	MAXIMUM RATING	UNIT
INPUT DIODE			
Power Dissipation	P_D	75	mW
Continuous Forward Current	I_F	50	mA
Reverse Voltage	V_R	5	V
OUTPUT PHOTOTRANSISTOR			
Power Dissipation	P_C	100	mW
Collector-Emitter Voltage	V_{CEO}	30	V
Emitter-Collector Voltage	V_{ECO}	5	V
Collector Current	I_C	20	mA
Operating Temperature Range	T_{opr}	-25℃ to + 85℃	
Storage Temperature Range	T_{stg}	-55℃ to + 100℃	
Lead Soldering Temperature [1.6mm (.063") Form Case]	T_{sol}	260℃ for 5 Seconds	

LITEON LITE-ON TECHNOLOGY CORPORATION

Property of Lite-On Only

ELECTRICAL OPTICAL CHARACTERISTICS AT T_A=25℃

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
INPUT DIODE							
Forward Voltage		V_F		1.2	1.6	V	I_F = 20mA
Reverse Current		I_R			100	μ A	V_R=5V
OUTPUT PHOTOTRANSISTOR							
Collector-Emitter Dark Current		I_{CEO}			100	nA	V_{CE}=10V
COUPLER							
Collector-Emitter Saturation Voltage		$V_{CE(SAT)}$			0.4	V	I_C=0.25mA If=20mA
On State Collector Current		$I_{C(ON)}$	0.5			mA	V_{CE}=5V I_F=20mA
Response Time	Rise Time	T_R		3	15	μ S	V_{CE}=5V, I_C=2mA R_L=100 Ω
	Fall Time	T_F		4	20		

TYPICAL ELECTRICAL / OPTICAL CHARACTERISTICS CURVES

(25℃ Ambient Temperature Unless Otherwise Noted)

Fig.1 Power Dissipation vs. Ambient Temperature

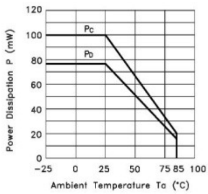


Fig.2 Forward Current vs. Forward Voltage

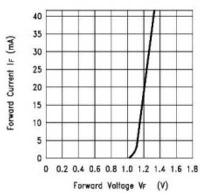


Fig.3 Cllector Current vs. Collector-emitter Voltage

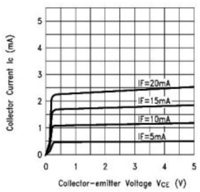
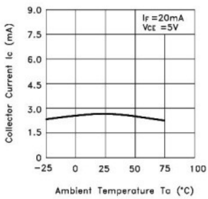


Fig.4 Collector Current vs. Ambient Temperature



LITEON **LITE-ON TECHNOLOGY CORPORATION**

Property of Lite-On Only

TYPICAL ELECTRICAL / OPTICAL CHARACTERISTICS CURVES

(25℃ Ambient Temperature Unless Otherwise Noted)

Fig.5 Collector–emitter Saturation Voltage vs. Ambient Temperature

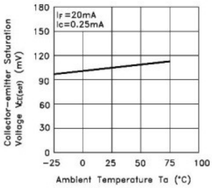
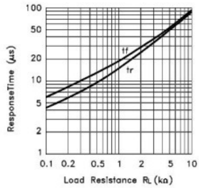


Fig.6 Response Time vs. Load Resistance



Test Circuit for Response Time